Amendments to the Specification:

Please replace paragraph beginning on page 2, line 19 with the following amended paragraph:

Referring to Figure 1, shown is a block diagram of a system 10 having a processor 12 that may include one or more registers 18 and 22. In this example, one register is called the control register 18 and the other register is called the main register 22. Each register 18 or 22 has a storage associated with it that provides an indicator. Thus, the main register 22 includes a main register update (MUP) bit storage 24 and the control register 18 includes a control register update (CUP) bit storage 20.

Please replace paragraph beginning on page 4, line 3 with the following amended paragraph:

A check at diamond 36 determines whether a context change has occurred. If so, control passes to block 38, where flow transitions to Figure 3 at which the CUP and MUP bits are checked, as indicated in block 40 in Figure 3. A check at diamond 42 determines whether the bit for the register that is going through a context change is set, indicating that the register has been changed. If so, the memory 16 may be updated as indicated in block 44. In the case where a single bit indicates whether any of a plurality of registers has been changed, all of the registers may be written to memory when any of the registers has changed. This may avoid the complexity of checking whether any of a large number of registers with a small amount of data have changed.